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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,444	12/15/2003	Ching-Chun Huang	NAUP0523USA	1443

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,444	HUANG ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in combination with Nishida et al. US Pub. 2001/0036705 A1 and Abadeer et al. US Pub. 2005/0090049 A1, and Parat et al. US Pub. 2004/0058508 A1 in combination with Kim et al. US Pub. 2004/0147090 A1.

The applicant's admitted prior art teaches STI are used for separation of HV-MOS and submicron-MOS in fig. 2. The applicant's admitted prior art does not disclose STI for the field oxide 58, 62.

The Nishida et al. reference discloses "trench isolation method is... an indispensable element isolation forming method to achieve higher density of semiconductor integrated circuits" [0005].

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the STI for the isolation region 58, 62 of the applicant's admitted prior art because the STI of Nishida et al. would provide the isolation regions with higher density achievement.

Further, the Abadeer et al. reference discloses in fig. 4 the use of STI with drift region 40/42 beneath the STI 41 can be used to substitute the FOX such as 210 of fig. 2 in the formation of high-voltage MOS transistor having STI region. The substrate is of a first conductive type, a deep well region is of a second conductive type, the first conductive type and the second conductive type are opposite to each other, [0024], [0031], e.g.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the teaching of combination with a trench and its drift region of Abadeer et al. because the device formation of Abadeer et al. would provide the combination with a drift region at the STI "to equally distribute the applied drain voltage laterally across the silicon surface in the drift region of the device" so that "high-power applications ... possess lower "on" resistance, faster switching speed, and lower gate drive power dissipation" (Abadeer et al.'s [0004]-[0005]).

The combination does not disclose formation of different-depth trenches.

The Parat et al. reference discloses an optimized method for forming shallow and deeper isolation trenches in a substrate comprising:

a) forming a pad oxide 113 on the surface of the substrate 110;

b) forming a silicon nitride layer 112 on a surface of the pad oxide layer 113;

c) forming a first hard mask 120 patterns on a surface of the silicon nitride layer 112;

d) performing a first etching process to remover portions of the silicon nitride layer and the substrate not covered by the first hard mask patterns to form a plurality of shallow trenches 125;

e) forming a second hard mask 128 patterns on the surface of the silicon nitride layer 112; and

f) performing a second etching process to remove portions of the silicon nitride layer and the substrate not covered by the second hard mask patterns to form a plurality of shallow trenches 130.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the combination trenches with the different-depth trenches formation as taught by Parat et al. because the different-depth trenches formation of Parat et al. would provide the trenches of the combination with the solution for critical dimensions of the different active regions of devices wherein deeper trenches would "sufficiently deep to adequately isolate neighboring devices" (Parat's [0005]).

The combination does not disclose formation of trenches filled with silicon oxide having the shape of a mushroom at the top of the trenches.

The Kim et al. reference discloses a method for forming isolation structures on a semiconductor substrate comprising:

a) forming a pad oxide 104 on the surface of the substrate 102;

b) forming a silicon nitride layer 106 on a surface of the pad oxide layer 104;

c) forming a first hard mask 108 patterns on a surface of the silicon nitride layer 106;

g) performing an isotropic etching process [0028] to remover portions 122 of the silicon nitride layer 106 along an interface of the pad oxide layer 104 and the silicon nitride layer 106;

h) forming a silicon oxide layer 150 on the surface of the substrate, and the silicon oxide layer filling up the shallow trenches 118;

i) performing a chemical mechanical polishing process to remove the silicon oxide layer 150 above a top surface of the silicon nitride layer 106 so that a top surface of the silicon oxide layer is aligned with the top surface of the silicon nitride layer, fig. 5; and

j) removing the silicon nitride layer 106 to have the tops of the silicon oxide layers in the shape of a mushroom, fig. 6.

The method further comprises a step for forming a linear oxide layer 126 in an inner surface of the shallow trenches after performing the isotropic etching process [0032]. A thickness of the silicon nitride layer 107 removed by the isotropic etching process is 200 angstroms [0032]. The silicon oxide layer 150 is formed by performing a CVD process [0035]. The wells are formed [0036]. The formed silicon oxide layers having the tops in the shape of a mushroom is to prevent a kink effect [0004].

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of Parat et al. with the further steps (steps g-j) of Kim et al. because the further steps of Kim et al. would provide the process of Parat et al. with

shoulders of the STI to prevent grooves around the STI that cause current problems. Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of Kim et al. with the steps of Parat et al. (steps d-f) because the steps of Parat et al. would provide the process of Kim et al. with both shallow and deeper trenches on the same substrate "to adequately isolate neighboring devices".

Further, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the combination of applicant's admitted prior art and Abadeer et al./Nishida et al. with the method of making trenches with different depths having the silicon oxide layers being in the shaped of a mushroom of the Parat et al. and Kim et al. combination because the mushroom-in-different-depth trenches would provide the combination of applicant's admitted prior art and Abadeer et al./Nishida et al. with a mean "to adequately isolate neighboring devices" and "prevent current problem".

Allowable Subject Matter

3. Claims 6 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art, individually or in combination, does not disclose or suggest all of the claimed elements in the present application wherein the two isolation ion

implantation regions are formed underneath the isolation shallow trenches to isolate the two active regions in the context of claims 3/20 and 1/15.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

05/27/2005

George Fourson
Primary Examiner